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(54) Jitter circuits; assessing jitter performance

(57) The jitter circuits comprise a jitter generator and a jitter detector in which jitter signals are synchronously associated with transmitted or received data patterns. This permits the performance of data transmission systems to be assessed with particular regard to the way in which particular data patterns affect the systems tolerance to jitter.

In Fig. 1, jitter information from a store 1 is used to impart jitter to a reference frequency which clocks data from a further store 6. The "jittered" data pattern is applied to a transmission system under test.

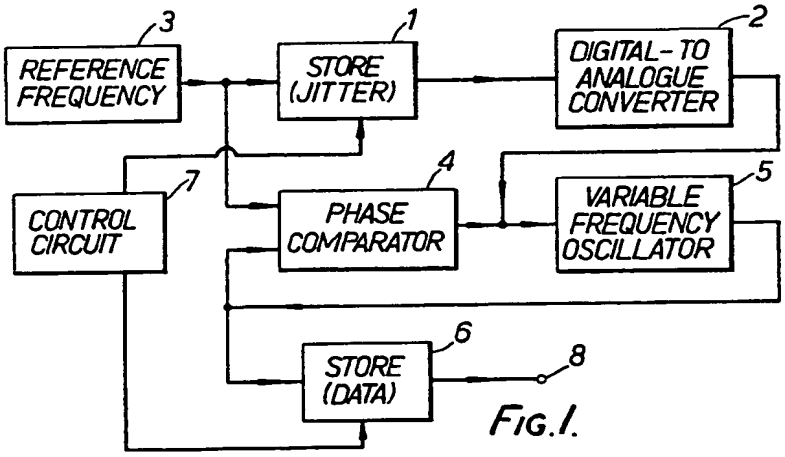

FIG. 1.

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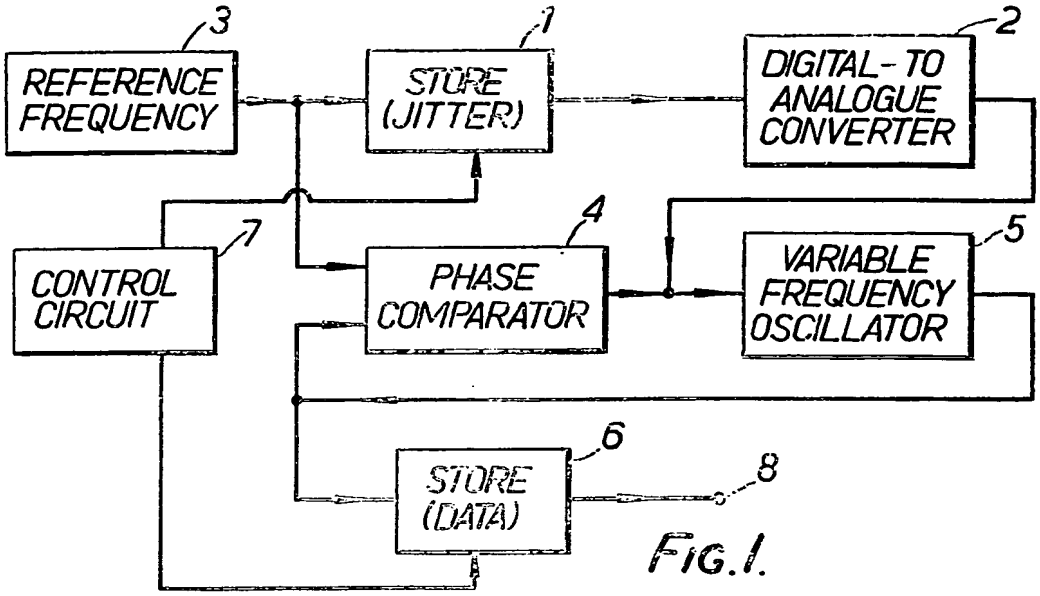

FIG. 1.

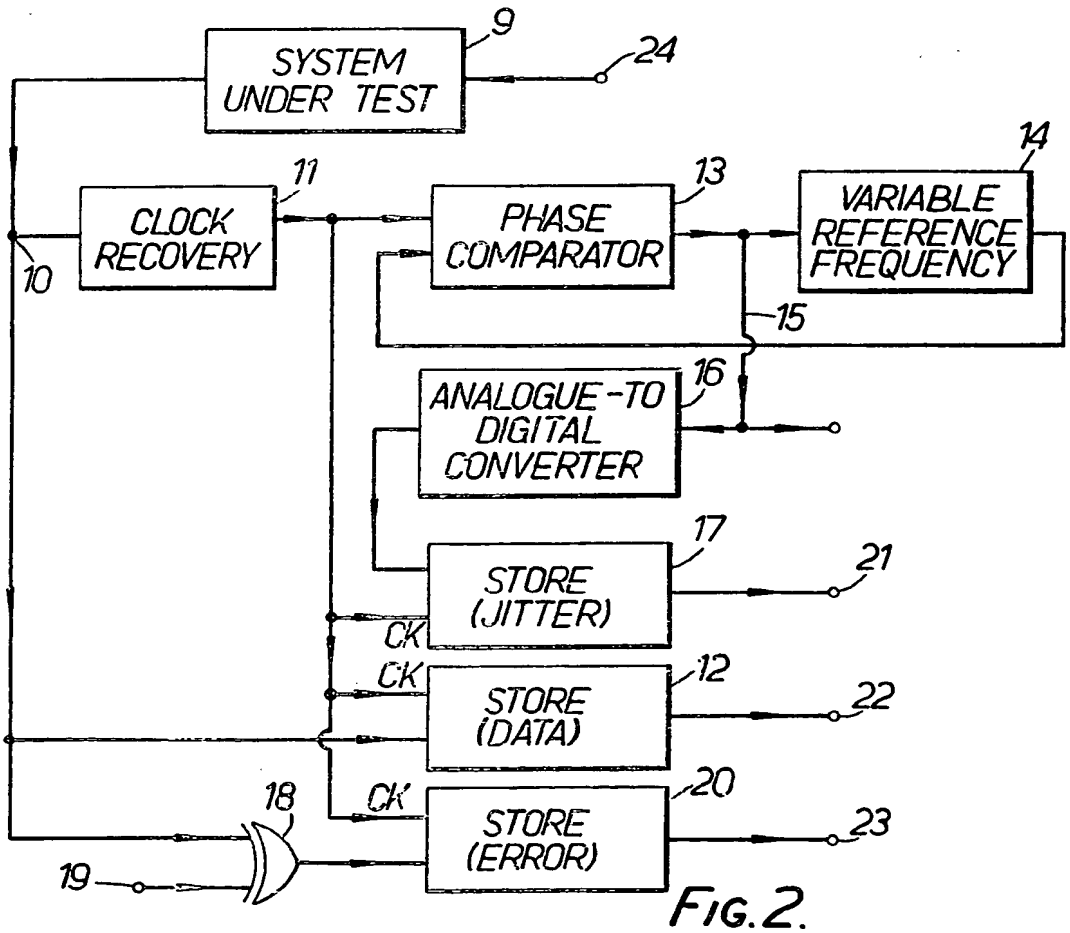

FIG. 2.

SPECIFICATION

Jitter circuits

This invention relates to jitter circuits, and is particularly concerned with jitter generators and/or detectors which enable the effect of signal jitter on a signal transmission system to ge evaluated. Many signal transmission systems, such as a data communication system, are designed to operate even if the transmitted signals are contaminated by jitter; jitter in this context being fluctuations in the timing of the signals with respect to their nominal or expected times of occurrence. In order to test and evaluate the way in which jitter will degrade the performance of transmission systems, it has been proposed to combine a test signal with a quantified uncorrelated jitter and to inject the composite signal into the system, and then to monitor the extent to which the test signal is corrupted as it passes through the system. Such procedures have been found to give inadequate results.

The present invention seeks to provide an improved jitter generator and/or jitter detector.

According to a first aspect of this invention, a jitter generator includes a source of jitter information having a predetermined characteristic and consisting of a known repeatable sequence of digital values; and means for combining the jitter information with a repeatable data pattern toproduce a composite output signal in which the jitter information is synchronised in a predetermined manner with a data pattern.

According to a second aspect of this invention, a jitter detector includes means for receiving a composite signal comprising a data pattern and a jitter signal; and means for extracting the jitter signal in a manner which permits identification of variations therein to be identified with particular portions of the data pattern.

The invention stems partly from the realisation that the susceptibility to jitter of a data transmission system depends not only on the nature of the jitter signals to which it is subjected, but also on the nature of the data which is passing through it and the way in which the jitter combines with the data pattern. For example, jitter often varies in a pseudo-random manner so as to give overall a measurable peak-to-peak timing variation, but it will include within it great variations in the rate at which the jitter alters. Many data transmission systems are less tolerant of some data sequence than others, so that whilst some data sequences may pass through the system without the introduction of errors, other data sequences under similar conditions may be quite severely corrupted. It will therefore be appreciated that the response of a data communicatin system to a jittered data pattern will depend upon the point-to-point variation of the data pattern and the jitter signal.

By correlating the jitter with its associated data pattern, very precise and repeatable measurements can be performed, and moreover, the tolerance of a system to specific jittered data sequences can be investigated indetail.

The invention is further described by way of example in which:

Figure 1 illustrates a jitter generator in accordance with the invention, and

Figure 2 illustrates a jitter receiver in combination with a system under test.

Referring to Fig. 1, a jitter generator is shown therein which is capable of generating a signal having a predetermined data pattern consisting of a stream of digital bits upon which is superimposed a jitter signal having predetermined characteristcs. The characteristics can be defined in terms of the peak-to-peak timing variations which can occur in the data pattern and/or the maximum rate at which the occurrence of timing edges can alter. A predetermined pattern of jitter information is held within a store 1 and is clocked out to a digital-to-analogue converter 2 under the control of a clock signal derived from a reference frequency source 3. The reference frequency is also applied to one input of a dual phase comparator 4. The output of the phase comparator is combined with the output of the digital-to-analogue converter 2 so that the stored jitter is superimposed upon the reference frequency 3 and the combined signal is fed via a low pass filter (not shown) to control the frequency of a variable frequency oscillator 5. As the output of the oscillator 5 is fed back to the other input of the phase comparator 4, the effect of the output frequency 5 is one of a nominal or centre frequency which is essentially the same as the reference frequency of the source 3, but which is modified in phase in accordance with the jitter information in store 1. Thus, instead of the pulse transitions occurring at regularly and predictably spaced intervals, they occur in a fashion which is determined by the jitter information such that the actual pulse edges occur at instants in time which in general depart from the regular period of the reference clock signal.

The variable frequency oscillator can be used to clock the store 1, instead of the reference frequency source, as both operate at nominally the same frequency.

The output of the variable frequency oscillator 5 is fed to a further store 6 which holds a predetermined pattern of data, usually binary data, which is to be encoded and fed into a system under test so as to permit an evaluation of the system.

In order to ensure that the data is fed out from the store 6 in repeatable synchronism

with the jitter held in store 1, both stores are operated under the control of a central circuit 7 which ensures that both stores commence reading information out, either simultaneously or delayed relative to one another by a precisely known and recorded amount.

The composite signal which is made available at terminal 8 therefore consists of a typical pattern of data which is mixed with a jitter signal having a predetermined characteristic. In a sense, the effect of the jitter information is to distort or corrupt the data pattern, but it is affected in a manner which is entirely predictable and repeatable. It can be determined by close inspection if required, which particular data bits are delayed or advanced by particular periods of time as represented by variations in the jitter signal. Thus, by associating particular levels of jitter with groups of data bits or sequences which are thought to be particularly troublesome to a system under test, its tolerance to jitter can be rapidly established under specified worst case operating conditions. Furthermore, the susceptibility of a system under test to particular data patterns can be assessed by subjecting selected portions of the data pattern todifferent levels of jitter. In principle, a system under test should be able to accept all possible data patterns without degrading them if it is operated in accordance with its own specification, but obviously it will be operating nearer its limits of performance on some data sequences rather than others.

The most satisfactory of data communication systems introduce jitter, i.e. timing errors, themselves, even if the original input signal which is applied to them is nominally of a perfect and uncorrupted nature.

The detector shown in Fig. 2 permits the level of jitter emerging from the system under test represented by block 9, to be correlated with the data pattern which is emerging from it simultaneously, sothat any relationship between the two can be accurately assessed. In principle, external jitter canbe applied to a system under test and correlated with data passing through it and any errors generated by it or, alternatively, just the internally generated jitter can be evaluated.

Referring to Fig. 2, a signal emanating from the data transmission system under test is received at terminal 10 of a jitter detector and this signal consists of a data pattern, normally an encoded binary data pattern in which the pulse transitions of the data are corrupted by the presence of jitter. It is necessary to first recover the internal clock frequency of the received signal in order to permit the data held within the signal to be decoded and extracted. A conventional clock recovery circuit 11 is used for this purpose and the recovered clock signal is used to clock the received data into a store 12 where it is temporarily held. The recovered clock signal, which still contains the incoming phase jitter, is applied to one input of a dual phase comparator 13, the output of which is fed via a low pass filter (not shown) to a variable reference frequency oscillator 14 so as to control the frequency thereof. In practice, the oscillator 14 is likely to be a crystal controlled device having only a limited amount of frequency variation, but this is normally sufficient to accommodate acceptable system variations. The oscillator 14 incorporates a low pass filter (not shown). The output of the oscillator 14 is fed back to the input of phase comparator 13. The effect of this is that the output of the phase comparator 13 contains a signal whose amplitude varies in accordance with the jitter present, and this signal is applied over lead 15 to an analogue-to-digital converter 16, the digital output of which is entered into a jitter store 17, which is clocked by the clock signal from the clock recovery circuit 11. Alternatively, it could be clocked by the variable frequency oscillator 5, as both are at the same frequency.

The effect of the jitter on the input signals is to cause errors in the transmission of the data pattern, and by comparing the data pattern with an original reference pattern which was initially applied to a system under test, the presence and occurrence of the errors can be precisely indicated. Thus, the incoming data is also applied to an exclusive-OR gate 18 which receives a reference pattern at terminal 19. If the reference pattern is identical with the received data, one particularly binary state (e.g. a logic 0) is entered into an error store 20, but if the recovered data disagrees with the reference pattern, the other binary state (e.g. a logic 1) is entered into the store 20 so as to record the existence of an error. The store 10 is clocked in the same way as store 17.

As the three sets of information, i.e. jitter information, the data pattern and the error information, are all held in three separate stores, and the elements of all three are related to the same clock frequency, the three sets can be examined and compared on a bit-by-bit basis to determine the degree of correspondence between them. If required, the three sets of information can be output on the three terminals 21, 22 and 23 for subsequent detailed analysis and correlation as required. If desired, a data pattern having a known jitter characteristic can be injected via terminal 24 into the system-under-test 9, and the effect on the data as it passes through the system can be monitored, and in this case the input signal is derived from the generator shown in Fig. 1. Alternatively, a jitter-free signal can be injected into terminal 24 so that the extent to which the system-under-test 9 introduces itself can be determined.

CLAIMS

1. A jitter generator including a source of jitter information having a predetermined characteristic and consisting of a known repeatable sequence of digital values; and means for combining the jitter information with a repeatable data pattern to produce a composite output signal in which the jitter information is synchronised in a predetermined manner with the data pattern.

2. A generator as claimed in claim 1 and wherein the jitter information is held in a store, from which it is arranged to read out under the control of a stable clock signal to constitute a jittered clock signal.

3. A generator as claimed in claim 2, and wherein the jittered clock signal is used to read out a data pattern from a further store so that the jitter is superimposed upon the data pattern.

4. A generator as claimed in claim 3, and wherein means are provided for shifting in time the data pattern relative to the jitter information by predetermined amounts.

5. A jitter detector including means for receiving a composite signal comprising a data pattern and a jitter signal; and means for extracting the jitter signal in a manner which permits identification of variations therein to be identified with particular portions of the data pattern.

6. A detector as claimed in claim 5, and wherein the jitter signal is extracted from the composite signal and is stored, the associated data pattern is also being extracted from the composite signal and stored in synchronism with the jitter signal to permit correlation with the jitter signal.

7. A detector as claimed in claim 6, and wherein means are provided for identifying errors in said data pattern, and for recording the presence of the errors in such a way as to permit correlation with those portions of the jitter signal which are associated with occurrence of the errors.

8. A method of evaluating a signal transmission system by monitoring its output by means of a jitter detector as claimed in claim 5, 6 or 7.

9. A method of evaluating a signal transmission system by applying to it a signal produced by a jitter generator as claimed in claim 1, 2, 3 or 4, and by monitoring the resultant output by means of a jitter detector as claimed in claim 5, 6 or 7.

10. A jitter generator substantially as illustrated in and described with reference to Fig. 1 of the accompanying drawing.

11. A jitter detector substantially as illustrated in and described with reference to Fig. 2 of the accompanying drawing.

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